

FEATURES

- Bidirectional Voltage Translator
- 2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DBQ, DW, NS, OR PW PACKAGE (TOP VIEW) V_{CCA} $\begin{bmatrix} 1 & 24 \\ 1 & 24 \end{bmatrix}$ V_{CCB}

DIR 2 23 🛛 NC A1 3 22 OE A2 🛛 4 21 B1 A3 🛛 5 20 B2 A4 🛛 6 19 B3 18 B4 A5 🛛 7 A6 🛛 8 17 B5 A7 | 9 16 П В6 15 B7 A8 10 GND 11 14 B8 GND [12 13 GND

NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB} , which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA} , which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, from a 2.5-V to a 3.3-V system environment and vice versa.

The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, \overline{OE}) is powered by V_{CCA}.

ORDERING INFORMATION

T _A	PACKAG	GE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC - DW	Tube of 25	SN74LVCC3245ADW	LVCC3245A
	30IC - DW	Reel of 2000	SN74LVCC3245ADWR	LV003243A
	SOP – NS	Reel of 2000	SN74LVCC3245ANSR	LVCC3245A
4000 to 0500	SSOP – DB	Reel of 2000	SN74LVCC3245ADBR	LH245A
–40°C to 85°C	SSOP (QSOP) – DBQ	Reel of 2500	SN74LVCC3245ADBQR	LVCC3245A
		Tube of 60	SN74LVCC3245APW	
	TSSOP – PW	Reel of 2000	SN74LVCC3245APWR	LH245A
		Reel of 250	SN74LVCC3245APWT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH TRANSCEIVER)

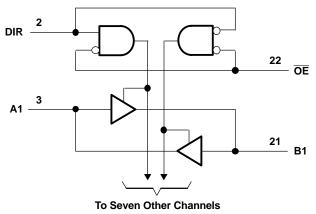
INP	UTS	OPERATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Х	Isolation



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SCAS5850-NOVEMBER 1996-REVISED MARCH 2005

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CCA} V _{CCB}	Supply voltage range		-0.5	6	V
		All A ports ⁽²⁾	-0.5	V _{CCA} + 0.5	
VI	Input voltage range	All B ports ⁽³⁾	-0.5	V _{CCB} + 0.5	V
		Except I/O ports ⁽²⁾	-0.5	V _{CCA} + 0.5	
V	$O_{\rm intrust violations rongo}(3)$	All A ports	-0.5	V _{CCA} + 0.5	V
Vo	Output voltage range ⁽³⁾	All B ports	-0.5	V _{CCB} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V_{CCA} , V_{CCB} , or	GND		±100	mA
		DB package		63	
		DBQ package		61	
θ_{JA}	Package thermal impedance ⁽⁴⁾	DW package		46	°C/W
		NS package		65	
		PW package		88	
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) This value is limited to 4.6 V maximum.

(3) This value is limited to 6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

SCAS5850-NOVEMBER 1996-REVISED MARCH 2005

Recommended Operating Conditions⁽¹⁾

V	Supply voltage	V _{CCA}	V _{CCB}	MIN 2.3	NOM 3.3	MAX 3.6	UNIT V
V _{CCA}				2.3	3.3 5		V
V _{CCB}	Supply voltage	2.2.1/	3 V		5	5.5	V
		2.3 V		1.7 2			
V _{IHA}	High-level input voltage	2.7 V 3 V	3 V 3.6 V	2			V
		3.6 V	5.5 V	2			
		2.3 V	3.5 V	2			
		2.3 V 2.7 V	3 V 3 V	2			
V _{IHB}	High-level input voltage	2.7 V 3 V	3.6 V	2			V
		3.6 V	5.5 V	3.85			
		2.3 V	5.5 V 3 V	3.60		0.7	
V _{ILA}	Low-level input voltage	2.7 V	3 V			0.8	V
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
		2.3 V 2.7 V	3 V			0.8	
V _{ILB}	Low-level input voltage		3 V			0.8	V
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			1.65	
		2.3 V	3 V	1.7			
V _{IH}	High-level input voltage (control pins) (referenced to V _{CCA})	2.7 V	3 V	2			V
	(referenced to V _{CCA})	3 V	3.6 V	2			
		3.6 V	5.5 V	2			
		2.3 V	3 V			0.7	
VIL	Low-level input voltage (control pins)	2.7 V	3 V			0.8	V
	(referenced to V _{CCA})	3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
VIA	Input voltage			0		V _{CCA}	V
V _{IB}	Input voltage			0		V _{CCB}	V
V _{OA}	Output voltage			0		V_{CCA}	V
V _{OB}	Output voltage			0		V _{CCB}	V
		2.3 V	3 V			-8	
I _{OHA}	High-level output current	2.7 V	3 V			-12	mA
ONA	3	3 V	3 V			-24	
		2.7 V	4.5 V			-24	
		2.3 V	3 V			-12	
I _{ОНВ}	High-level output current	2.7 V	3 V			-12	mA
Опр	5	3 V	3 V			-24	
		2.7 V	4.5 V			-24	
		2.3 V	3 V			8	
I _{OLA}	Low-level output current	2.7 V	3 V			12	mA
·OLA		3 V	3 V			24	
		2.7 V	4.5 V			24	

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SCAS5850-NOVEMBER 1996-REVISED MARCH 2005



Recommended Operating Conditions (continued)

		V _{CCA}	V _{CCB}	MIN NOM	MAX	UNIT
		2.3 V	3 V		12	
		2.7 V	3 V		12	
IOLB	Low-level output current	3 V	3 V		24	mA
		2.7 V	4.5 V		24	
$\Delta t / \Delta v$	Input transition rise or fall rate				10	ns/V
T _A	Operating free-air temperature			-40	85	°C

SCAS5850-NOVEMBER 1996-REVISED MARCH 2005

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	UNIT
		I _{OH} = -100 μA	3 V	3 V	2.9	3		
		$I_{OH} = -8 \text{ mA}$	2.3 V	3 V	2			
N/		1. 10	2.7 V	3 V	2.2	2.5		V
V _{OHA}		$I_{OH} = -12 \text{ mA}$	3 V	3 V	2.4	2.8		V
			3 V	3 V	2.2	2.6		
		$I_{OH} = -24 \text{ mA}$	2.7 V	4.5 V	2	2.3		
		I _{OH} = -100 μA	3 V	3 V	2.9	3		
		40.54	2.3 V	3 V	2.4			
V _{OHB}		$I_{OH} = -12 \text{ mA}$	2.7 V	3 V	2.4	2.8		V
			3 V	3 V	2.2	2.6		
		$I_{OH} = -24 \text{ mA}$	2.7 V	4.5 V	3.2	4.2		
		I _{OL} = 100 μA	3 V	3 V			0.1	
		$I_{OL} = 8 \text{ mA}$	2.3 V	3 V			0.6	
V _{OLA}		$I_{OL} = 12 \text{ mA}$	2.7 V	3 V		0.1	0.5	V
			3 V	3 V		0.2	0.5	
		I _{OL} = 24 mA	2.7 V	4.5 V		0.2	0.5	
		I _{OL} = 100 μA	3 V	3 V			0.1	
		$I_{OL} = 12 \text{ mA}$	2.3 V	3 V			0.4	
V _{OLB}			3 V	3 V		0.2	0.5	V
		I _{OL} = 24 mA	2.7 V	4.5 V		0.2	0.5	
				3.6 V		±0.1	±1	
I _I	Control inputs	$V_{I} = V_{CCA}$ or GND	3.6 V	5.5 V		±0.1	±1	μA
I _{OZ} ⁽¹⁾	A or B ports	$V_{O} = V_{CCA/B}$ or GND, $V_{I} = V_{IL}$ or V_{IH}	3.6 V	3.6 V		±0.5	±5	μA
-		A port = V_{CCA} or GND, $I_0 = 0$	3.6 V	Open		5	50	
I _{CCA}	B to A			3.6 V		5	50	μA
		B port = V_{CCB} or GND, $I_0 = 0$	3.6 V	5.5 V		5	50	
				3.6 V		5	50	_
I _{CCB}	A to B	A port = V_{CCA} or GND, $I_0 = 0$	3.6 V	5.5 V		8	80	μA
	A port	$V_{I} = V_{CCA} - 0.6 \text{ V}$, Other inputs at V_{CCA} or GND, OE at GND and DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	
$\Delta I_{CCA}^{(2)}$	ŌĒ	$V_{I} = V_{CCA} - 0.6 \text{ V}$, Other inputs at V_{CCA} or GND, DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	DIR	$V_{\rm L} = V_{\rm CCA} - 0.6$ V, Other inputs at V _{CCA} or GND, OE at GND	3.6 V	3.6 V		0.35	0.5	
$\Delta I_{CCB}^{(2)}$	B port	$V_{\rm L}$ = V _{CCB} – 2.1 V, Other inputs at V _{CCB} or GND, OE at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
Ci	Control inputs	$V_{I} = V_{CCA}$ or GND	Open	Open		4		pF
C _{io}	A or B ports	$V_{O} = V_{CCA/B}$ or GND	3.3 V	5 V		18.5		pF

(1)

For I/O ports, the parameter I_{OZ} includes the input leakage current. This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V_{CC}. (2)



SCAS5850-NOVEMBER 1996-REVISED MARCH 2005

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCA} = ± 0.2 V _{CCB} = ± 0.3	V, 3.3 V	V _{CCA} = 2. 3.6 V V _{CCB} = ± 0.5	/, 5 V	V _{CCA} = 2. 3.6 V V _{CCB} = 2. 1.0 V C _{CCB} = 2. ± 0.3	V, 3.3 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PHL}	А	В	1	9.4	1	6	1	7.1	20
t _{PLH}	A	D	1	9.1	1	5.3	1	7.2	ns
t _{PHL}	В	А	1	11.2	1	5.8	1	6.4	20
t _{PLH}	D	A	1	9.9	1	7	1	7.6	ns
t _{PZL}	OE	•	1	14.5	1	9.2	1	9.7	
t _{PZH}	UE	A	1	12.9	1	9.5	1	9.5	ns
t _{PZL}	ŌĒ	P	1	13	1	8.1	1	9.2	
t _{PZH}	UE	В	1	12.8	1	8.4	1	9.9	ns
t _{PLZ}	ŌĒ	•	1	7.1	1	7	1	6.6	
t _{PHZ}	UE	A	1	6.9	1	7.8	1	6.9	ns
t _{PLZ}	ŌĒ	P	1	8.8	1	7.3	1	7.5	
t _{PHZ}	UE	В	1	8.9	1	7	1	7.9	ns

Operating Characteristics

 $V_{CCA} = 3.3 \text{ V}, V_{CCB} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST C	ONDITIONS	TYP	UNIT
~		Outputs enabled	0 50		38	
C _{pd}	Power dissipation capacitance per transceiver	Outputs disabled	$C_{L} = 50,$	f = 10 MHz	4.5	р⊦

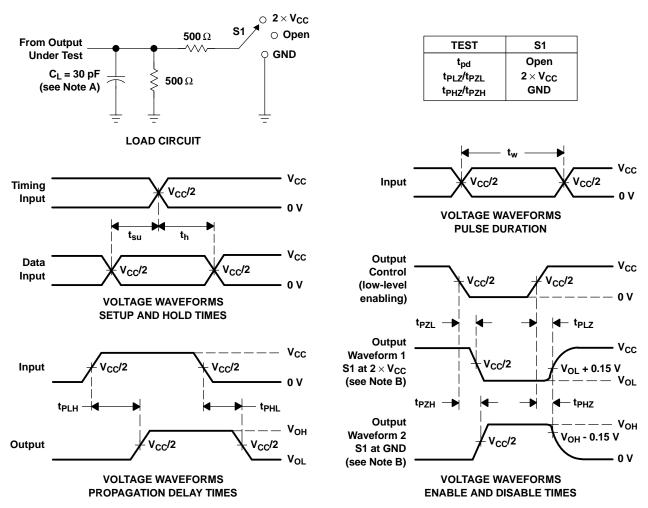
Power-Up Considerations⁽¹⁾

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. To guard against such power-up problems, take these precautions:

- 1. Connect ground before any supply voltage is applied.
- 2. Power up the control side of the device (V_{CCA} for all four of these devices).
- 3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
- 4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.
- (1) Refer to the TI application report, Texas Instruments Voltage-Level-Translation Devices, literature number SCEA021.

SCAS5850-NOVEMBER 1996-REVISED MARCH 2005





NOTES: A. CL includes probe and jig capacitance.

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- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

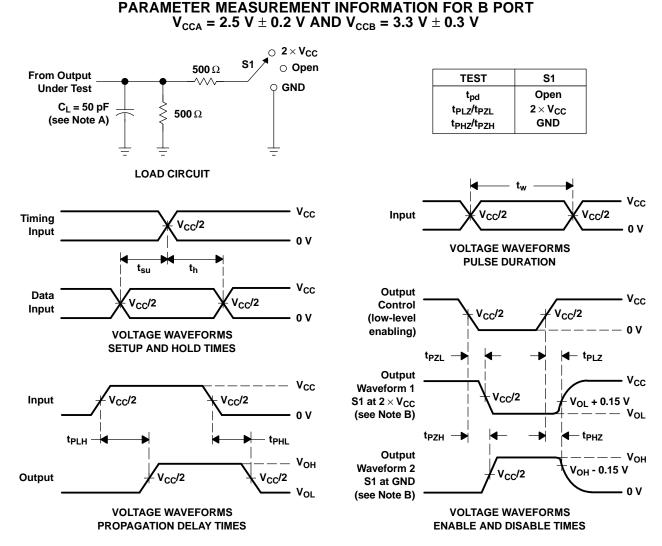
Figure 1. Load Circuit and Voltage Waveforms



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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

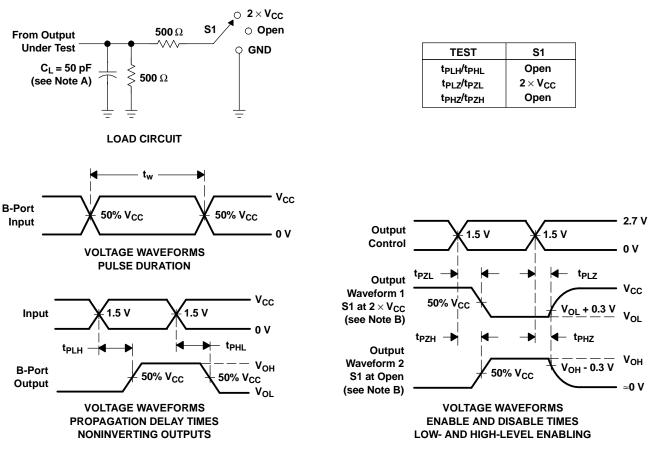
Figure 2. Load Circuit and Voltage Waveforms

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SN74LVCC3245A OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION FOR B PORT V_{CCA} = 3.6 V and v_{CCB} = 5.5 V

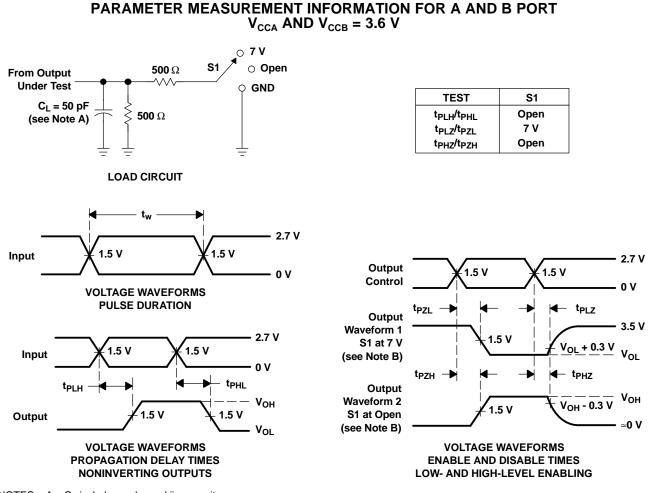


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_r \leq 2.5 ns. t_f \leq 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms



SCAS5850-NOVEMBER 1996-REVISED MARCH 2005



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan ⁽²⁾	Lead/Ball Finisl	n MSL Peak Temp ⁽³⁾
74LVCC3245ADBQRE4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74LVCC3245ADBQRG4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LVCC3245ADBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74LVCC3245ADBQR	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LVCC3245ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ANSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245ANSRG4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245APWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245APWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245APWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74LVCC3245APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245APWTE4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCC3245APWTG4	ACTIVE	TSSOP	PW	24	250	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM
	-	-		-				





Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
					no Sh/Br)		

no Sb/Br)

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVCC3245A :

Enhanced Product: SN74LVCC3245A-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCC3245ADBQR	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCC3245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ANSR	SO	NS	24	2000	330.0	24.4	8.2	15.4	2.5	12.0	24.0	Q1
SN74LVCC3245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCC3245ADBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
SN74LVCC3245ADBR	SSOP	DB	24	2000	346.0	346.0	33.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	346.0	346.0	41.0
SN74LVCC3245ANSR	SO	NS	24	2000	346.0	346.0	41.0
SN74LVCC3245APWR	TSSOP	PW	24	2000	346.0	346.0	33.0

MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



MECHANICAL DATA

MTSS001C - JANUARY 1995 - REVISED FEBRUARY 1999

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.

D. Falls within JEDEC MO-137 variation AE.



DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AD.



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